Remarks

The Applicants enclose a new Fig. 1 which is marked as "Prior Art" in accordance with the Examiner's helpful suggestion. Entry of the replacement drawing into the official file is respectfully requested.

The Specification has been amended in accordance with the Examiner's helpful suggestion with respect to "EDGA" which has been changed to "EDFA." Withdrawal of the objection is respectfully requested.

Claims 33, 39 and 44 are rejected over several minor grammatical and typographical errors. Each of those claims has been amended in accordance with the Examiner's helpful suggestion. Withdrawal of the objection to those claims is respectfully requested.

Claims 24 and 46 have been amended to place them into better condition for allowance. For example, Claim 24 has been amended to recite that the monochrome transmitters have a slave local clock. Support may be found in the Applicants' Specification in paragraph [0043]. Claim 24 has also been amended to recite the step of formatting the multiplexed signal by an optical gate. Support may be found in the Applicants' Specification in paragraph [0041]. Claim 24 has further been amended to recite that each slave local clock from each transmitter is controlled by a synchronization circuit comprising a master clock and a phase locked loop (PLL), the master clock controlling the clock of the optical gate and each slave clock by using the phase locked loop which supplies the synchronization for each of the transmitters. Support may be found in the Applicants' Specification in paragraphs [0041] and [0048]. Entry of that change into the official file is respectfully requested.

Claim 46 has been amended to recite a plurality of monochrome transmitters, each of which has its own transmission wavelength, which each transmitter having a slave clock. Support may be found throughout the Applicants' Specification such as at paragraph [0025] and elsewhere. Entry into the official file is respectfully requested.

Claims 24-32 stand rejected under 35 U.S.C. §102 as being anticipated by Bosotti. The Applicants note with appreciation the Examiner's detailed comments hypothetically applying Bosotti to those claims. The Applicants nonetheless respectfully submit that Bosotti fails to disclose, either explicitly or implicitly, all of the features recited in Claims 24-32. Reasons are set forth below.

Bosotti discloses reducing the interference phenomenon between adjacent channels in a multi-channel telecommunications system, causing parasite superposition effects of these signals

from adjacent channels. Bosotti synchronizes each carrying information issued by the transponders so that the peaks of the signals reach the demultiplexer such that any pair of spectrally adjacent channels lags by half of a signal period of their data flow or the fastest data flow among the two data streams.

Thus, Bosotti discloses a common clock to control the signals from each transmitter to synchronize them. However, the timing is not a phase alignment of the signals, but instead is a shift of the same phases of the half of a signal period between two adjacent channel signals. This is sharply contrasted to Claims 24-32 wherein the master clock (or the PLL) is connected to each transmitter clock, but also to the clock to the optical gate, the optical gate being arranged before a possible demultiplexer. The Applicants' device is indeed synchronizing equipment and a counter-reaction loop to synchronize the signals before transmitting the multiplexed signal on the transmission line.

However, in Bosotti, the master clock is connected only to fit each phase of each transmitter, the transmitter also being able to be connected to a phase shift controller, itself being connected to a phase shift detector in the output of the demultiplexer. Thus, Bosotti uses no counter-reaction loop between the multiplexer and the transmission line. Yet that is the feature that provides a quality signal before transmitting on the transmission line.

The Applicants therefore respectfully submit that the subject matter of the Claim 24 differs from Bosotti in that the multiplexed signal is formatted through an optical gate and the synchronization circuit also includes a common master clock and a phase locked loop, the master clock controlling the clock of the optical gate and each slave clock by using the phase locked loop which provides a synchronization signal to each transmitter. These distinctive features achieve an enslavement method for phase auto-fitting of input signals of an external modulator. Withdrawal of the rejection based on Bosotti is respectfully requested.

Claims 38 and 39 stand rejected under 35 U.S.C. §102 as being anticipated by Yoshifuji. The Applicants again appreciate the Examiner's comments with respect to the theoretical application of Yoshifuji to Claims 38 and 39. The Applicants again respectfully submit that Yoshifuji fails to explicitly or implicitly disclose all of the subject matter recited in those two claims. Reasons are set forth below.

Yoshifuji discloses equipment for point-to-point transmission typical of the prior art, i.e., including a set of transmitters that each can transmit a signal from a different wavelength in the direction of a multiplexer (col. 1, lines 26-31). Yoshifuji also discloses the possibility of using an optical ring on the transmission line to detect and treat errors on the transmission line to avoid a shutdown of transmission. For this purpose, several slave stations are used, each station including a local slave clock. These slave clocks are driven by the master clock of the master station.

However, this system is based on an optical ring and arranged on the transmission line, and not based on a counter-reaction loop with transmitters. Indeed, the subject matter of Claims 38 and 29 make it possible to deliver a quality signal in the output of the multiplexer, transmission errors on the line being not taken into account. In particular, the elements controlled by a master clock are slave stations which are not transmitters. Transmitters of the device do not include local clocks, each of which is connected to a master clock. Moreover, the transmission does not occur on a single transmission line, but on several.

Thus, Yoshifuji discloses equipment to be implemented on a transmission line, which is contrary to the subject matter of Claims 38 and 39 on equipment upstream of the transmission line. Claims 38 and 39 differ from Yoshifuji in that the clock master controls slave clocks of each one of these transmitters. Withdrawal of the rejection based on Yoshifuji is respectfully requested.

Claim 46 stands rejected under 35 U.S.C. §102 as being anticipated by Mussino. The Applicants respectfully submit, however, that Mussino fails to explicitly or implicitly disclose all of the subject matter set forth in that claim. Reasons are set forth below.

Mussino discloses a method for analog modulating of an optical signal. That method also implements a marker ("pilot tone") in the form of a sinusoidal signal with predetermined amplitude and frequency, and a presence detector in the optical signal in the output of disruptions of the such marked signal (col. 1, lines 59-67). However, Mussino only discloses marking a single signal from one transmitter, not a plurality of signals in a multi-channel system.

Thus, Claim 46 differs from Mussino because the disturbing signal is injected on each transmitter and the output detection means are arranged at an optical gate.

The implementation of these distinctive features is not accessible to one skilled in the art. Injection of a disturbing signal on each transmitter and the arrangement of the output detection means at an optical gate allow each transmitter to be enslaved in a multi-channel system. This

advantage is not by Mussino since the injection of a disturbing signal on each transmitter and the arrangement of the output detection means at an optical gate are simply not disclosed. Withdrawal of the rejection based on Mussino is respectfully requested.

Claims 33-37 stand rejected under 35 U.S.C. §103 over the hypothetical combination of Mussino with Bosotti. The Applicants respectfully submit that even if one skilled in the art were to hypothetically combine those two disclosures, the process resulting from that combination would be different from what the Applicants claim.

The distinctive features of Claims 33-37 are not disclosed in Mussino. Implementation of these distinctive features is not obvious to one skilled in the art because nothing guides the skilled person in the art from Bosotti or in combination with Mussino, to use a common clock controlling both an optical gate arranged after the multiplexer, and each transmitter. As a result, Claims 33-37 are non-obvious regarding Bosotti and Mussino, taken separately or in combination. Withdrawal of the rejection of Claims 33-37 based on the combination of Mussino with Bosotti is respectfully requested.

Claims 40-44 stand rejected under 35 U.S.C. §103 over the hypothetical combination of Mussino with Yoshifuji. The Applicants respectfully submit that the combination of Mussino with Yoshifuji would still result in structure different from what the Applicants recite in Claims 40-44. Reasons are set forth below.

The feature according to which the master clock controls the slave clocks of each one of the transmitters is not disclosed in Mussino and cannot be deduced from a combination with Yoshifuji. Implementation of a master clock connected to each transmitter would lead to achieve a counter-reaction loop between the output and the input of each transmitter, and not between the multiplexer output and each transmitter according to Claims 40-44. Yet, that is the feature that provides the advantage of pooling signals from each transmitter. This advantage is not disclosed by Mussino with Yoshifuji or from general knowledge of one skilled in the art because their combination does not provide the advantage of Claims 40-44 by achieving the control by the master clock in this way. Withdrawal of the rejection based on the combination of Mussino with Yoshifuji is respectfully requested.

Claim 45 stands rejected under 35 U.S.C. §103 over the hypothetical combination of Takeuchi with Yoshifuji. The Applicants respectfully submit that this combination would also not

result in the Applicants' claimed apparatus. In that regard, the Applicants already established the inapplicability of Yoshifuji. Takeuchi fails to disclose that the master clock controls the slave clocks as each of the transmitters. Thus, hypothetically combining Takeuchi with Yoshifuji is substantially the same as attempting to combine Mussino with Yoshifuji. The result is something completely different from what the Applicants recite in Claim 45. Withdrawal of that rejection is also respectfully requested.

In light of the foregoing, the Applicants respectfully submit that the entire Application is now in condition for allowance, which is respectfully requested.

Respectfully submitted,

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In the Drawings

Kindly replace Fig. 1 now of record with new Fig. 1 attached herewith.